

ABSTRACT OF THE DISCLOSURE

A sacrificial, self-aligned polysilicon interconnect structure is formed in a region of insulating material to the side of an active region location and underlying a semiconductor device of a substrate assembly in order to electrically connect the active region and the semiconductor device. A method for making the interconnect structure maintains a preexisting geometry of the active region during etching of an interconnect structure hole in which the interconnect structure is formed and saves process steps. Under the method, a region of insulating material is formed immediately adjacent the active region location. A nitride layer is formed over the active region and protects the active region while an interconnect structure hole is etched partially into the region of insulating material adjacent the active region location with an etching process that is selective to the nitride layer. The interconnect structure hole is filled with polysilicon, the surface of the substrate assembly is planarized, and the nitride layer is removed.

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